



TFT LCD Preliminary Specification

MODEL NO.: N141C6 - L01

Customer:

Approved by:

Note:

記錄	工作	審核	角色	投票
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**REVISION HISTORY**

Version	Date	Page (New)	Section	Description
0.0	Jan 24, '08	All	All	Tentative specification was first issued.
1.0	Aug. 08, '08	All	All	Preliminary Specification was first issued.



1 GENERAL DESCRIPTION

1.1 OVERVIEW

N141C6 - L01 is a 14.1" TFT Liquid Crystal Display module with single LED Backlight unit and 50 pins LVDS interface. This module supports 1440 x (3 RGB) x 900 WXGA+ mode and can display 262,144 colors.

The optimum viewing angle is at 6 o'clock direction. The converter module for backlight is not built in.

1.2 FEATURES

- Thin and Light Weight
- WXGA+ (1440 x 900 pixels) resolution
- DE only mode
- 3.3V LVDS (Low Voltage Differential Signaling) interface with 2 pixel/clock
- RoHS compliance

1.3 APPLICATION

- TFT LCD Notebook

1.4 GENERAL SPECIFICATIONS

Item	Specification	Unit	Note
Active Area	303.48(H) X 189.675(V) (14.1 inch Diagonal)	mm	(1)
Bezel Opening Area	306.88 (H) x 193.075 (V)	mm	
Driver Element	a-si TFT active matrix	-	-
Pixel Number	1440 x R.G.B. x 900	pixel	-
Pixel Pitch	0.21075 (H) x 0.21075 (V)	mm	-
Pixel Arrangement	RGB vertical stripe	-	-
Display Colors	262,144	color	-
Transmissive Mode	Normally white	-	-
Surface Treatment	Anti-glare and Hard Coat , Haze 26, (3H min.)	-	-

1.5 MECHANICAL SPECIFICATIONS

Item		Min.	Typ.	Max.	Unit	Note
Module Size	Horizontal(H)	319	319.5	320	mm	(1)
	Vertical(V)	206	206.5	207	mm	
	Depth(D)	--	5.28	5.5	mm	
Weight		--	--	375	g	

Note (1) Please refer to the attached drawings for more information of front and back outline dimensions

2 ABSOLUTE MAXIMUM RATINGS

2.1 ABSOLUTE RATINGS OF ENVIRONMENT

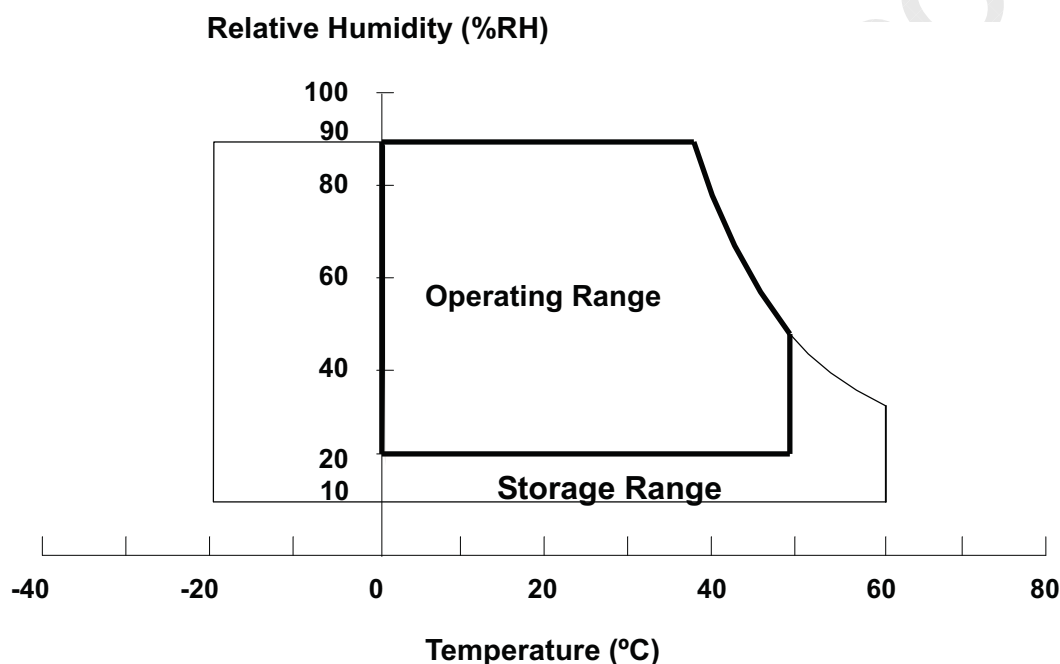
Item	Symbol	Value		Unit	Note
		Min.	Max.		
Storage Temperature	T _{ST}	-20	+60	°C	(1)
Operating Ambient Temperature	T _{OP}	0	+50	°C	(1), (2)
Shock (Non-Operating)	S _{NOP}	-	220/2	G/ms	(3), (5)
Vibration (Non-Operating)	V _{NOP}	-	1.5	G	(4), (5)

Note (1) (a) 90 %RH Max. (Ta ≤ 40 °C).

(b) Wet-bulb temperature should be 39 °C Max. (Ta > 40 °C).

(c) No condensation.

Note (2) The temperature of panel display surface area should be 0 °C Min. and 60 °C Max..

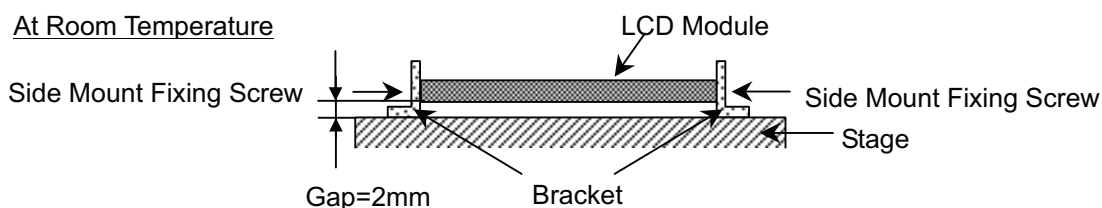


Note (3) 1 time for ± X, ± Y, ± Z. for Condition (220G / 2ms) is half Sine Wave,.

Note (4) 10 ~ 500 Hz, 30 min / Cycle, 1 cycles for each X, Y, Z axis.

Note (5) At testing Vibration and Shock, the fixture in holding the module has to be hard and rigid enough so that the module would not be twisted or bent by the fixture.

The fixing condition is shown as below:





2.2 ELECTRICAL ABSOLUTE RATINGS

2.2.1 TFT LCD MODULE

Item	Symbol	Value		Unit	Note
		Min.	Max.		
Power Supply Voltage	V_{CC}	-0.3	+4.0	V	(1)
Logic Input Voltage	V_{IN}	-0.3	$V_{CC}+0.3$	V	

2.2.2 BACKLIGHT UNIT

Item	Symbol	Value		Unit	Note
		Min.	Max.		
LED Light Bar Power Supply Voltage	V_L	0	3.3	V	(1), (2)
LED Light Bar Power Supply Current	I_L	0	30	mA	

Note (1) Permanent damage to the device may occur if maximum values are exceeded. Function operation should be restricted to the conditions described under Normal Operating Conditions.

Note (2) Specified values are for LED (Refer to 3.2 for further information).

3 ELECTRICAL CHARACTERISTICS

3.1 TFT LCD MODULE

 $T_a = 25 \pm 2^\circ\text{C}$

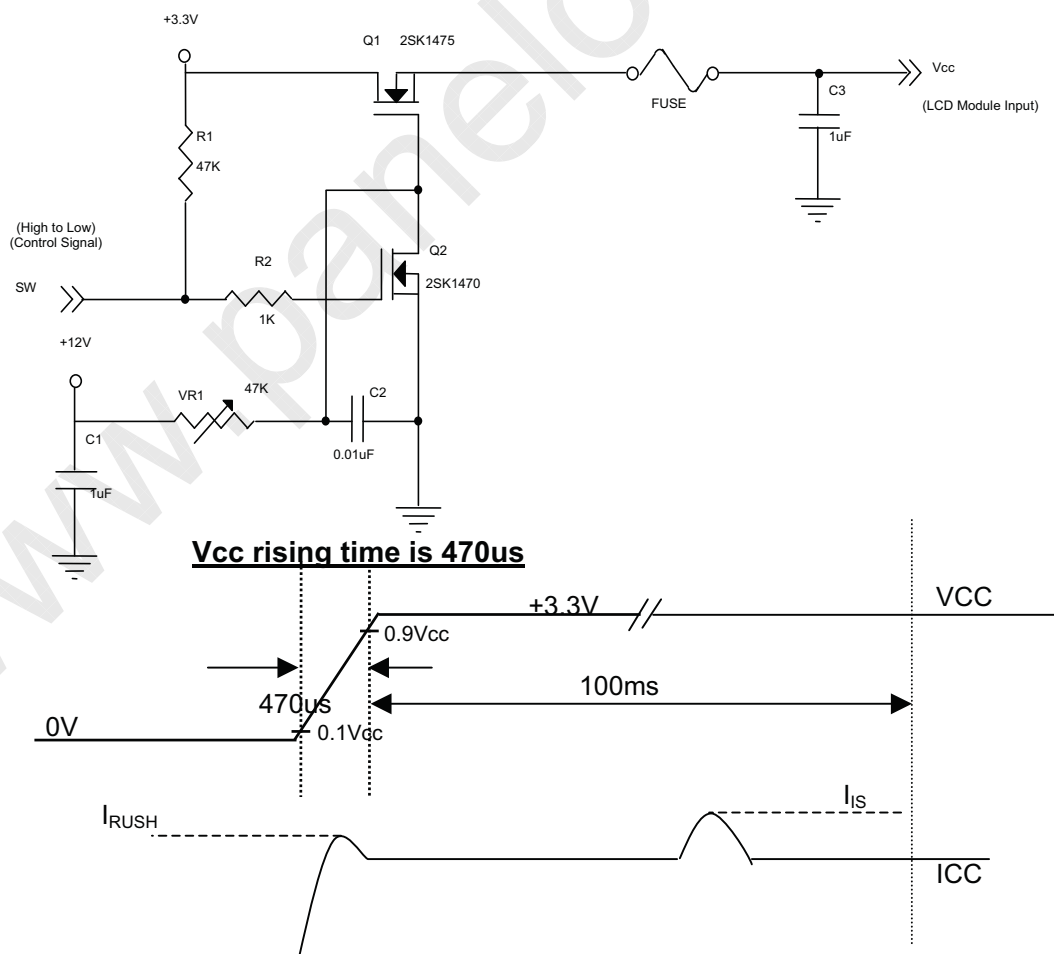
Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
Power Supply Voltage	V_{CC}	3.0	3.3	3.6	V	-
Permissible Ripple Voltage	V_{RP}		50		mV	-
Rush Current	I_{RUSH}			1.5	A	(2)
Initial Stage Current	I_{IS}			1.0	A	(2)
Power Supply Current	White		370		mA	(3)a
	Black		480		mA	(3)b
LVDS Differential Input High Threshold	$V_{TH(LVDS)}$			+100	mV	(5), $V_{CM}=1.2V$
LVDS Differential Input Low Threshold	$V_{TL(LVDS)}$	-100			mV	(5), $V_{CM}=1.2V$
LVDS Common Mode Voltage	V_{CM}	1.125		1.375	V	(5)
LVDS Differential Input Voltage	$ V_{ID} $	100		600	mV	(5)
Terminating Resistor	R_T		100		Ohm	
Power per EBL WG	P_{EBL}	-	2.0223	-	W	(4)

Note (1) The ambient temperature is $T_a = 25 \pm 2^\circ\text{C}$.

Note (2) I_{RUSH} : the maximum current when V_{CC} is rising

I_{IS} : the maximum current of the first 100ms after power-on

Measurement Conditions: Shown as the following figure. Test pattern: black



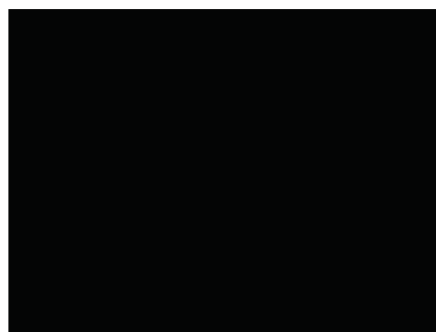
Note (3) The specified power supply current is under the conditions at $V_{CC} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$, whereas a power dissipation check pattern below is displayed.

a. White Pattern



Active Area

b. Black Pattern



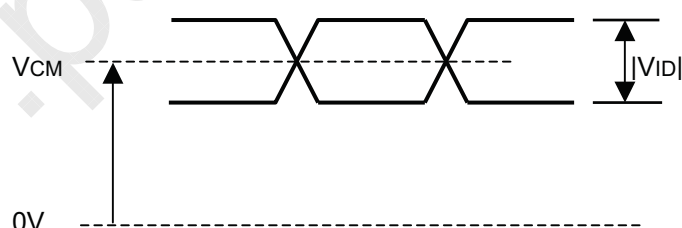
Active Area

Note (4) The specified power are the sum of LCD panel electronics input power and the converter input power. Test conditions are as follows.

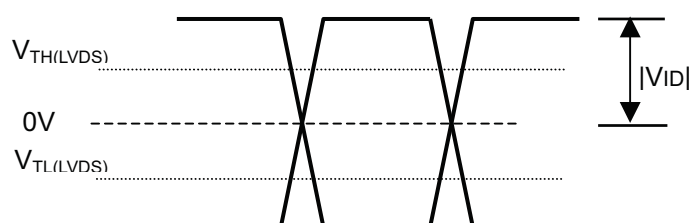
- (a) $V_{CC} = 3.3\text{ V}$, $T_a = 25 \pm 2\text{ }^{\circ}\text{C}$, $f_v = 60\text{ Hz}$,
- (b) The pattern used is a black and white 32 x 36 checkerboard, slide #100 from the VESA file "Flat Panel Display Monitor Setup Patterns", FPDMSU.ppt.
- (c) Luminance: 60 nits.
- (d) The inverter used is provided from TBD. Please contact them for detail information. CMO doesn't provide the inverter in this product.

Note (5) The parameters of LVDS signals are defined as the following figures.

Single Ended



Differential



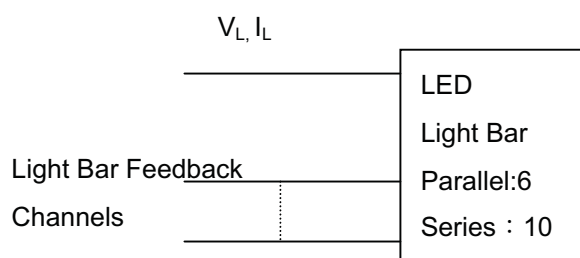


3.2 BACKLIGHT UNIT

Ta = 25 ± 2 °C

Parameter	Symbol	Value			Unit	Note
		Min.	Typ.	Max.		
LED Quantity		60			Pcs	(1),
LED light bar Power Supply Voltage	V _L	30	32	33	V _{dc}	(1), (2)
LED light bar Power Supply Current	I _L	--	102	150	mA	
LED Life Time	L _{BL}	15,000	-	-	Hrs	(4)
Power Consumption	Po	-	3.264	4.95	W	(3), I _L = 102.0 mA

Note (1) LED light bar configuration is shown as below:



Note (2) For better LED light bar driving quality, it is recommended to utilize the adaptive boost converter with current balancing function to drive LED light-bar.

Note (3) PO = IL × VL

Note (4) The lifetime of LED is defined as the time when it continues to operate under the conditions at Ta = 25 ±2 oC and IL = 17 mA(Per EA) until the brightness becomes ≤ 50% of its original value.



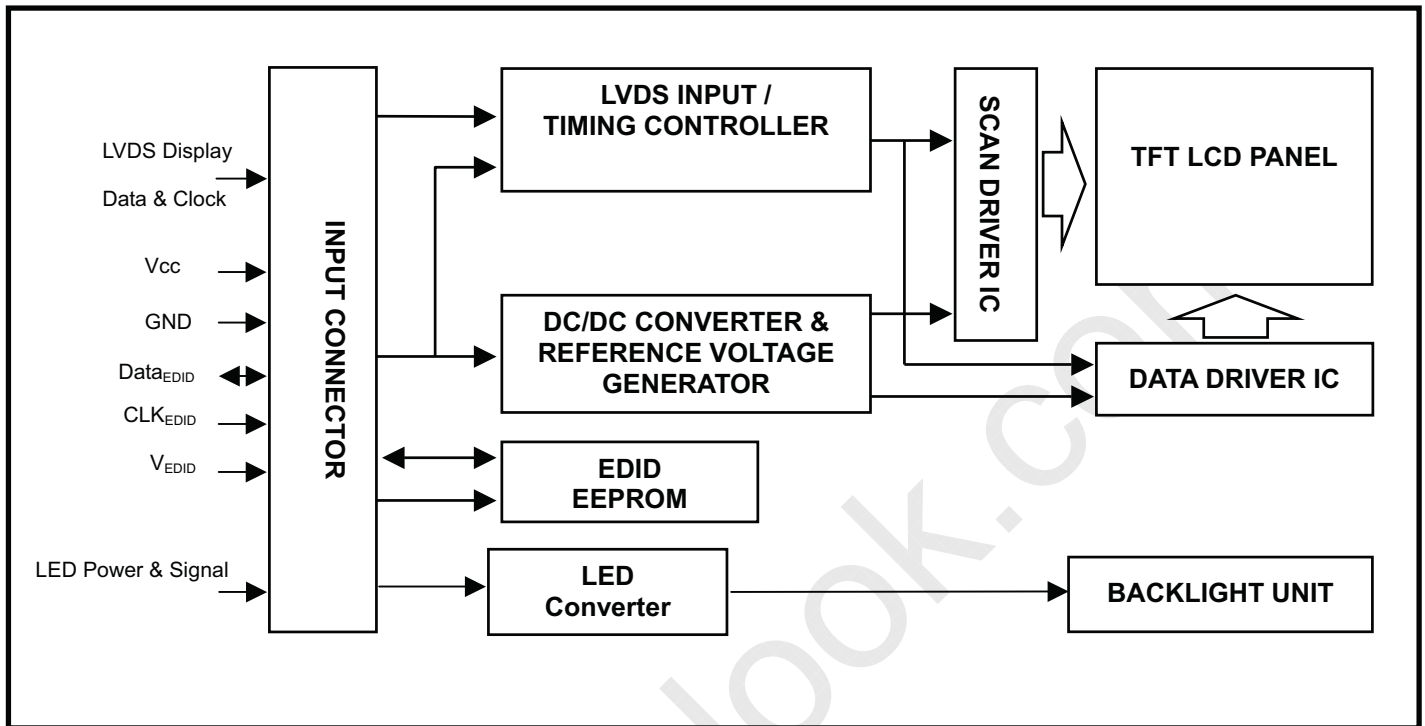
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OPTOELECTRONICS CORP.

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Issued Date: Aug. 08, 2008
Model No.: N141C6 - L01

Preliminary

4 BLOCK DIAGRAM

4.1 TFT LCD MODULE





5 INPUT TERMINAL PIN ASSIGNMENT

5.1 TFT LCD MODULE

Pin	Symbol	Description	Polarity	Remark
1	Test Loop	Test Loop (only to pin 30)		
2	VEDID	EDID 3.3V power		
3	VSS	Ground		
4	CLKEDID	EDID clock		
5	DATAEDID	EDID data		
6	VSS	Ground		
7	RXO0-	- LVDS differential data input (R0-R5, G0)	Negative	
8	RXO0+	+ LVDS differential data input (R0-R5, G0)	Positive	
9	VSS	Ground		
10	RinO1-	- LVDS differential data input (G1-G5, B0-B1) (Odd)	Negative	
11	RinO1+	+ LVDS differential data input (G1-G5, B0-B1) (Odd)	Positive	
12	VSS	Ground		
13	RinO2-	- LVDS differential data input (B2-B5, HS, VS, DE) (Odd)	Negative	
14	RinO2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (Odd)	Positive	
15	VSS	Ground		
16	RXOC-	- LVDS differential clock input (Odd)	Negative	
17	RXOC+	+ LVDS differential clock input (Odd)	Positive	
18	VSS	Ground		
19	RinE0-	- LVDS differential data input (R0-R5, G0) (Even)	Negative	
20	RinE0+	+ LVDS differential data input (R0-R5, G0) (Even)	Positive	
21	VSS	Ground		
22	RinE1-	- LVDS differential data input (G1-G5, B0-B1) (Even)	Negative	1.
23	RinE1+	+ LVDS differential data input (G1-G5, B0-B1) (Even)	Positive	
24	VSS	Ground		
25	RinE2-	- LVDS differential data input (B2-B5, HS, VS, DE) (Even)	Negative	
26	RinE2+	+ LVDS differential data input (B2-B5, HS, VS, DE) (Even)	Positive	
27	VSS	Ground		
28	RXEC-	- LVDS differential clock input (Even)	Negative	
29	RXEC+	+ LVDS differential clock input (Even)	Positive	
30	Test Loop	Test Loop (only to pin 1)		
31	CONNTST	Connector test (this pin connected to pin 50 only)		(1)
32	Vcc	Power Supply +3.3 V (typical)		
33	Vcc	Power Supply +3.3 V (typical)		
34	BIST	Panel Self Test		
35	NC	no connect		
36	VSS	Ground		
37	VSS	Ground		
38	PWM BL	PWM brightness control		
39	VBL-	Ground		
40	VBL-	Ground		
41	VBL-	Ground		
42	VBL-	Ground		
43	NC	no connect		
44	VBL+	7V – 20V LED power		LED Power Input
45	VBL+	7V – 20V LED power		
46	VBL+	7V – 20V LED power		
47	VBL+	7V – 20V LED power		
48	SMB_DATA	SMBus data		
49	SMB_CLK	SMBus clock		
50	CONNTST	Connector test (this pin to be connected to pin 31 only)		(1)



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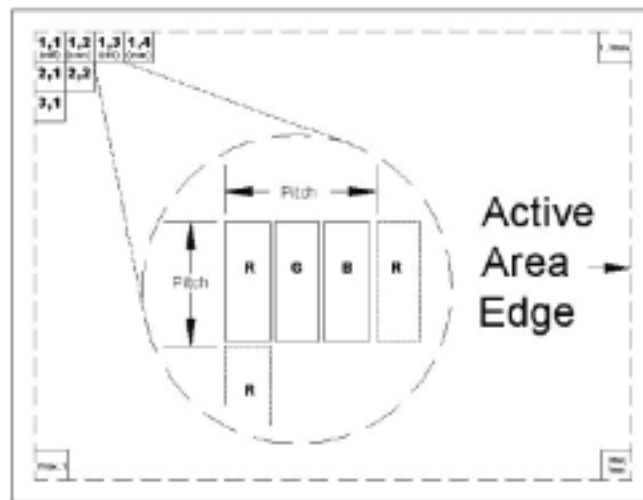
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Note (1) Connector Part No.: JAE-FI-VHP50S-A-HF11 or equivalent

Note (2) User's connector Part No: JAE-FI-X30C2L or equivalent

Note (3) The first pixel is odd as shown in the following figure.



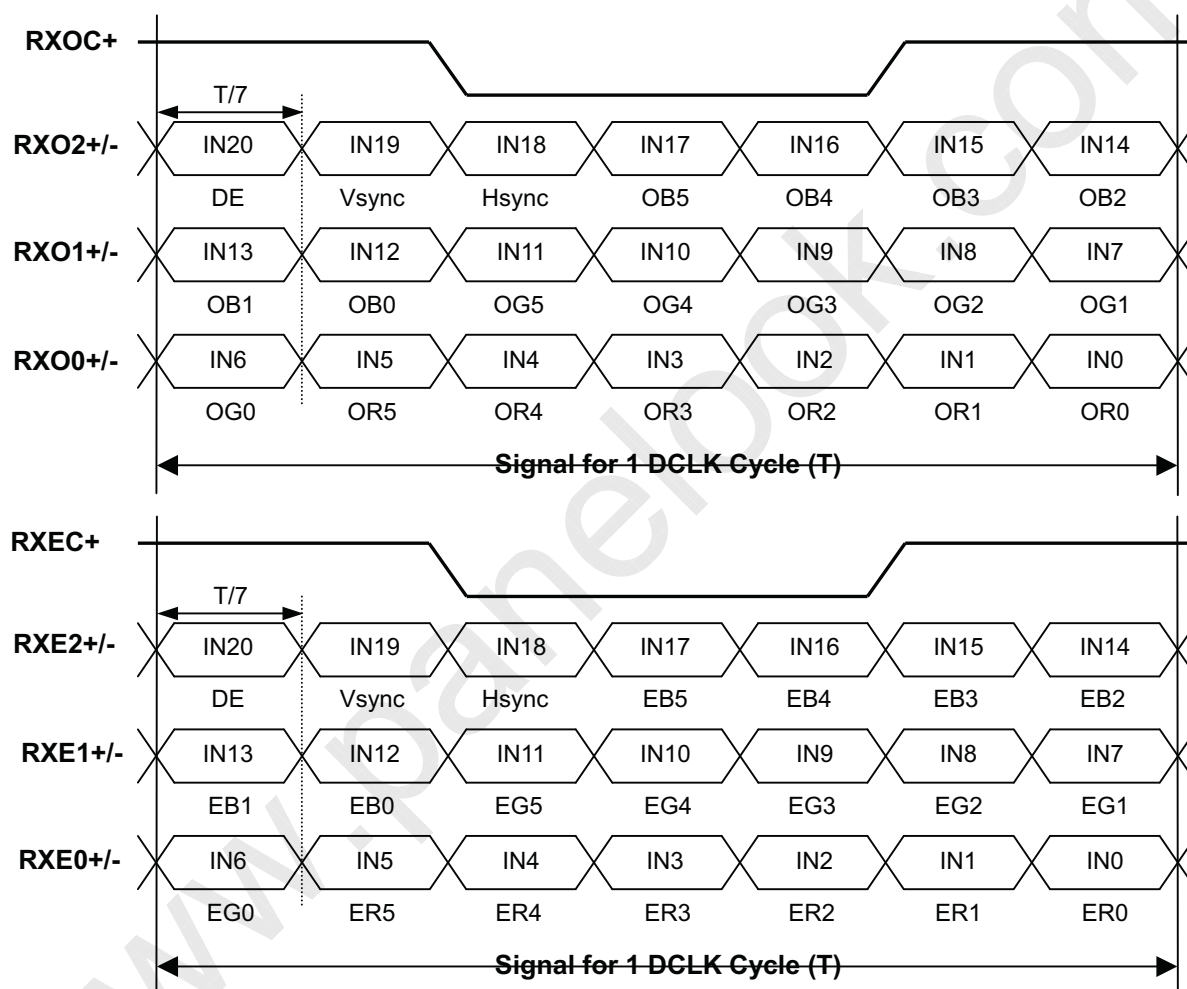
5.2 BACKLIGHT UNIT

Pin	Symbol	Description	Color
1	HV	High Voltage	Pink
2	LV	Ground	White

Note (1) Connector Part No.: FCI-59453-091110EDLF or equivalent

Note (2) User's connector Part No.: SM02B-BHSS-1-TB or equivalent

5.3 TIMING DIAGRAM OF LVDS INPUT SIGNAL



5.4 COLOR DATA INPUT ASSIGNMENT

The brightness of each primary color (red, green and blue) is based on the 6-bit gray scale data input for the color. The higher the binary input, the brighter the color. The table below provides the assignment of color versus data input.

Color		Data Signal																	
		Red						Green						Blue					
		R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
Basic Colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Cyan	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1
	Magenta	1	1	1	1	1	1	0	0	0	0	0	0	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray Scale Of Red	Red(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red(1)	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(2)	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:	:
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	Red(61)	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
	Red(62)	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0
Red(63)	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	
Gray Scale Of Green	Green(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Green(1)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Green(2)	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
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	Green(61)	0	0	0	0	0	0	1	1	1	1	0	1	0	0	0	0	0	0
	Green(62)	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0	0	0
Green(63)	0	0	0	0	0	0	1	1	1	1	1	1	0	0	0	0	0	0	
Gray Scale Of Blue	Blue(0)/Dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue(1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	Blue(2)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
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	Blue(61)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1
	Blue(62)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0
Blue(63)	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	

Note (1) 0: Low Level Voltage, 1: High Level Voltage



5.5 EDID DATA STRUCTURE

The EDID (Extended Display Identification Data) data formats are to support displays as defined in the VESA Plug & Display and FPD1 standards.

Byte # (decimal)	Byte (hex)	Field Name and Comments	Value (hex)	Value (binary)
0	0	Header	00	00000000
1	1	Header	FF	11111111
2	2	Header	FF	11111111
3	3	Header	FF	11111111
4	4	Header	FF	11111111
5	5	Header	FF	11111111
6	6	Header	FF	11111111
7	7	Header	00	00000000
8	8	EISA ID manufacturer name ("CMO")	0D	00001101
9	9	EISA ID manufacturer name (Compressed ASCII)	AF	10101111
10	0A	ID product code (N141C6-L01)	36	00110110
11	0B	ID product code (hex LSB first; N141C6-L01)	14	00010100
12	0C	ID S/N (fixed "0")	00	00000000
13	0D	ID S/N (fixed "0")	00	00000000
14	0E	ID S/N (fixed "0")	00	00000000
15	0F	ID S/N (fixed "0")	00	00000000
16	10	Week of manufacture	14	00010100
17	11	Year of manufacture	12	00010010
18	12	EDID structure version # ("1")	01	00000001
19	13	EDID revision # ("3")	03	00000011
20	14	Video I/P definition ("digital")	90	10010000
21	15	Active area horizontal 30.348cm	1E	00011110
22	16	Active area vertical 18.9675cm	13	00010011
23	17	Display Gamma (Gamma = "2.2")	78	01111000
24	18	Feature support ("Active off, RGB Color")	0A	00001010
25	19	Rx1 Rx0 Ry1 Ry0 Gx1 Gx0 Gy1 Gy0	87	10000111
26	1A	Bx1 Bx0 By1 By0 Wx1 Wx0 Wy1 Wy0	F5	11110101
27	1B	Rx=0.580	94	10010100
28	1C	Ry=0.340	57	01010111
29	1D	Gx=0.310	4F	01001111
30	1E	Gy=0.550	8C	10001100
31	1F	Bx=0.155	27	00100111
32	20	By=0.155	27	00100111
33	21	Wx=0.313	50	01010000
34	22	Wy=0.329	54	01010100
35	23	Established timings 1	00	00000000
36	24	Established timings 2 (1440*900@60Hz)	00	00000000
37	25	Manufacturer's reserved timings	00	00000000
38	26	Standard timing ID # 1	01	00000001
39	27	Standard timing ID # 1	01	00000001
40	28	Standard timing ID # 2	01	00000001
41	29	Standard timing ID # 2	01	00000001
42	2A	Standard timing ID # 3	01	00000001
43	2B	Standard timing ID # 3	01	00000001



44	2C	Standard timing ID # 4	01	00000001
45	2D	Standard timing ID # 4	01	00000001
46	2E	Standard timing ID # 5	01	00000001
47	2F	Standard timing ID # 5	01	00000001
48	30	Standard timing ID # 6	01	00000001
49	31	Standard timing ID # 6	01	00000001
50	32	Standard timing ID # 7	01	00000001
51	33	Standard timing ID # 7	01	00000001
52	34	Standard timing ID # 8	01	00000001
53	35	Standard timing ID # 8	01	00000001
54	36	Detailed timing description # 1 Pixel clock ("88.75MHz", According to VESA CVT Rev1.1)	AB	10101011
55	37	# 1 Pixel clock (hex LSB first)	22	00100010
56	38	# 1 H active ("1440")	A0	10100000
57	39	# 1 H blank ("160")	A0	10100000
58	3A	# 1 H active : H blank ("1440 : 160")	50	01010000
59	3B	# 1 V active ("900")	84	10000100
60	3C	# 1 V blank ("26")	1A	00011010
61	3D	# 1 V active : V blank ("900 :26")	30	00110000
62	3E	# 1 H sync offset ("48")	30	00110000
63	3F	# 1 H sync pulse width ("32")	20	00100000
64	40	# 1 V sync offset : V sync pulse width ("3 : 6")	36	00110110
65	41	# 1 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 3 : 6")	00	00000000
66	42	# 1 H image size ("303 mm")	2F	00101111
67	43	# 1 V image size ("190 mm")	BE	10111110
68	44	# 1 H image size : V image size ("303 : 190")	10	00010000
69	45	# 1 H boarder ("0")	00	00000000
70	46	# 1 V boarder ("0")	00	00000000
71	47	# 1 Non-interlaced ; Normal display, no stereo ; Digital Separate ; V sync POL is negative ; H sync POL is positive	1A	00011010
72	48	Detailed timing description # 2 Pixel clock ("58.5MHz", According to VESA CVT Rev1.1)	DA	11011010
73	49	# 2 Pixel clock (hex LSB first)	16	00010110
74	4A	# 2 H active ("1440")	A0	10100000
75	4B	# 2 H blank ("160")	A0	10100000
76	4C	# 2 H active : H blank ("1440 : 160")	50	01010000
77	4D	# 2 V active ("900")	84	10000100
78	4E	# 2 V blank ("17")	11	00010001
79	4F	# 2 V active : V blank ("900 :17")	30	00110000
80	50	# 2 H sync offset ("48")	30	00110000
81	51	# 2 H sync pulse width ("32")	20	00100000
82	52	# 2 V sync offset : V sync pulse width ("3 : 6")	36	00110110
83	53	# 2 H sync offset : H sync pulse width : V sync offset : V sync width ("48: 32 : 3 : 6")	00	00000000
84	54	# 2 H image size ("303 mm")	2F	00101111
85	55	# 2 V image size ("190 mm")	BE	10111110
86	56	# 2 H image size : V image size ("303 : 190")	10	00010000
87	57	# 2 H boarder ("0")	00	00000000



88	58	# 2 V boarder ("0")	00	00000000
		# 2 Non-interlaced ; Normal display, no stereo ; Digital Separate ; V sync POL is negative ; H sync POL is positive	1A	00011010
89	59			
90	5A	Detailed timing description # 3	00	00000000
91	5B	# 3 Flag	00	00000000
92	5C	# 3 Reserved	00	00000000
93	5D	# 3 FE (hex) defines ASCII string (Model Name "N141C5", ASCII)	FE	11111110
94	5E	# 3 Flag	00	00000000
95	5F	# Dell P/N "NM050" 1 st character ("N")	4E	01001110
96	60	# Dell P/N "NM050" 1 st character ("M")	4D	01001101
97	61	# Dell P/N "NM050" 1 st character ("0")	30	00110000
98	62	# Dell P/N "NM050" 1 st character ("5")	35	00110101
99	63	# Dell P/N "NM050" 1 st character ("0")	30	00110000
100	64	LCD Supplier EEDID Revision #: "02"	82	10000010
101	65	Manufacturer P/N ("N")	4E	01001110
102	66	Manufacturer P/N ("1")	31	00110001
103	67	Manufacturer P/N ("4")	34	00110100
104	68	Manufacturer P/N ("1")	31	00110001
105	69	Manufacturer P/N ("C")	43	01000011
106	6A	Manufacturer P/N ("6")	36	00110110
107	6B	Manufacturer P/N (If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
108	6C	Flag	00	00000000
109	6D	Flag	00	00000000
110	6E	Flag	00	00000000
111	6F	Data Type Tag:	00	00000000
112	70	Flag	00	00000000
113	71	SMBUS value @ 10nits = 00	00	00000000
114	72	SMBUS value @ 17nits = 00	00	00000000
115	73	SMBUS value @ 24nits = 00	00	00000000
116	74	SMBUS value @ 30nits = 00	00	00000000
117	75	SMBUS value @ 60nits = 00	00	00000000
118	76	SMBUS value @ 110nits = 00	00	00000000
119	77	SMBUS value @ 160nits = 00	00	00000000
120	78	SMBUS value @ max nits = 00	00	00000000
		Bit[1:0] 00:reserved , 01: single LVDS, 10: dual LVDS, 11: reserved Bit[2] 0: No RTC support , 1: RTC support Bit[7:3] Reserved	02	00000010
121	79			
122	7A	BIST Enable: Yes = '01' No = '00' ("Yes")	01	00000001
123	7B	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	0A	00001010
124	7C	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
125	7D	(If <13 char, then terminate with ASCII code 0Ah, set remaining char = 20h)	20	00100000
126	7E	Extension flag	00	00000000
127	7F	Checksum	41	01000001



6 INTERFACE TIMING

(9).

IN

PUT SIGNAL TIMING SPECIFICATIONS

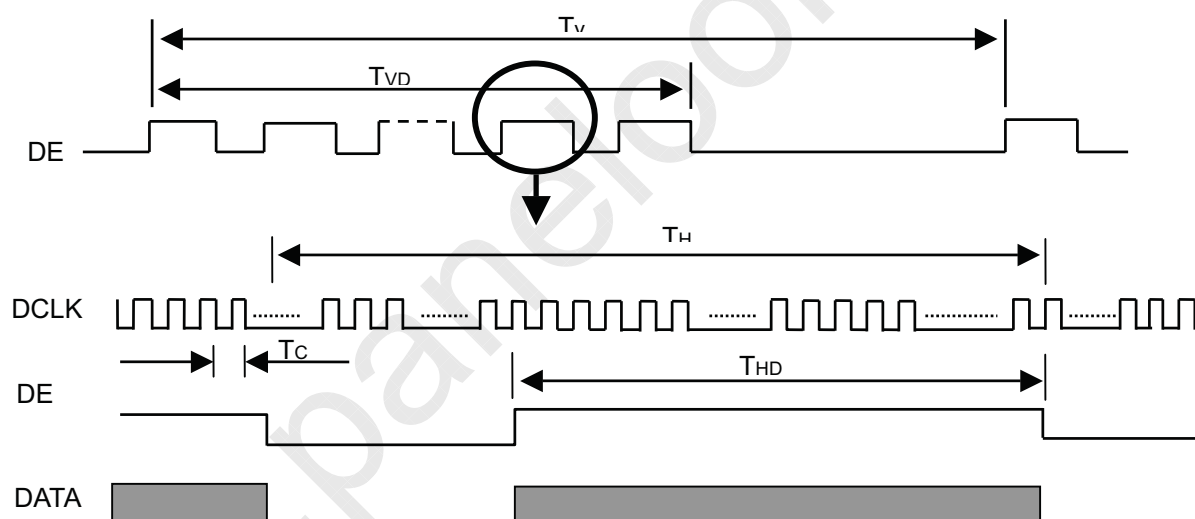
The specifications of input signal timing are as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	25	44.5	60	MHz	(2)
DE	Vertical Total Time	TV	910	926	1500	TH	-
	Vertical Active Display Period	TVD	900	900	900	TH	-
	Vertical Active Blanking Period	TVB	TV-TVD	26	TV-TVD	TH	
	Horizontal Total Time	TH	760	800	880	Tc	(2)
	Horizontal Active Display Period	THD	720	720	720	Tc	(2)
	Horizontal Active Blanking Period	THB	TH-THD	80	TH-THD	Tc	(2)

Note (1) Because this module is operated by DE only mode, Hsync and Vsync are ignored.

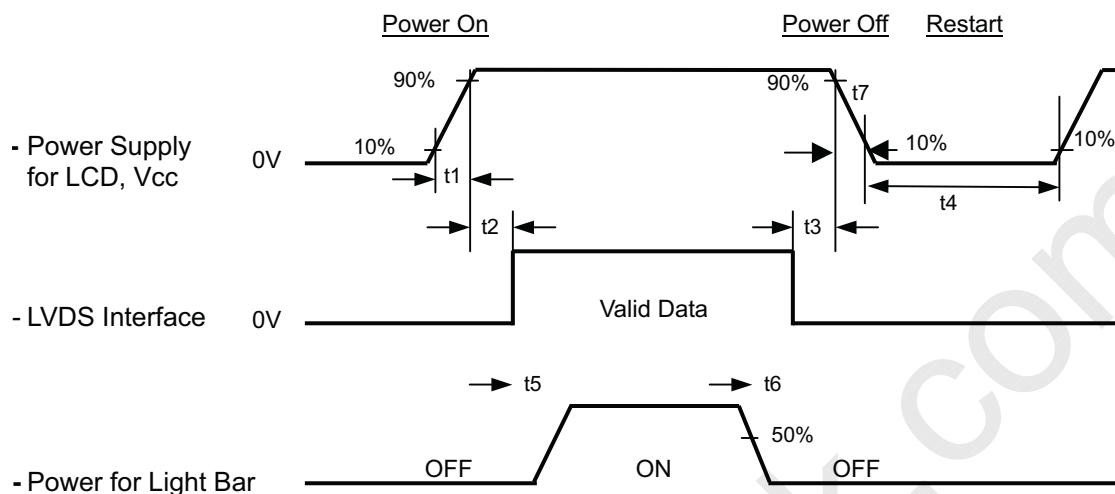
(2) 2 channels LVDS input.

INPUT SIGNAL TIMING DIAGRAM





6.2 POWER ON/OFF SEQUENCE



Timing Specifications:

$$0.5 < t_1 \leq 10 \text{ msec}$$

$$0 < t_2 \leq 50 \text{ msec}$$

$$0 < t_3 \leq 50 \text{ msec}$$

$$t_4 \geq 500 \text{ msec}$$

$$t_5 \geq 200 \text{ msec}$$

$$t_6 \geq 200 \text{ msec}$$

Note (1) Please follow the power on/off sequence described above. Otherwise, the LCD module might be damaged.

Note (2) Please avoid floating state of interface signal at invalid period. When the interface signal is invalid, be sure to pull down the power supply of LCD Vcc to 0 V.

Note (3) The Backlight inverter power must be turned on after the power supply for the logic and the interface signal is valid. The Backlight inverter power must be turned off before the power supply for the logic and the interface signal is invalid.

Note (4) Sometimes some slight noise shows when LCD is turned off (even backlight is already off). To avoid this phenomenon, we suggest that the Vcc falling time is better to follow $5 \leq t_7 \leq 300 \text{ ms}$.



7 OPTICAL CHARACTERISTICS

(9).

TE

ST CONDITIONS

Item	Symbol	Value	Unit
Ambient Temperature	Ta	25±2	°C
Ambient Humidity	Ha	50±10	%RH
Supply Voltage	V _{CC}	3.3	V
Input Signal	According to typical value in "3. ELECTRICAL CHARACTERISTICS"		
LED Light Bar Input Current	I _L	(102)	mA

The relative measurement methods of optical characteristics are shown in 7.2. The following items should be measured under the test conditions described in 7.1 and stable environment shown in Note (6).

7.2 OPTICAL SPECIFICATIONS

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Note
Contrast Ratio		CR	$\theta_x=0^\circ, \theta_y=0^\circ$ Viewing Normal Angle	400	--	-	-	(2), (6)
Response Time		T _R		-	5	10	ms	(3)
		T _F		-	11	16	ms	
Average Luminance of White		L _{AVE}		250	300	-	cd/m ²	(4), (6)
White Variation		δW5p		-	-	20	%	(5), (6)
		δW13p				35	%	
Color Gamut		C.G		42	45		%	(6), (7)
Color Chromaticity	Red	R _x		TBD	0.580	TBD	-	(1), (6)
		R _y			0.340		-	
	Green	G _x			0.310		-	
		G _y			0.550		-	
	Blue	B _x			0.155		-	
		B _y			0.155		-	
	White	W _x			0.313		-	
		W _y			0.329		-	
Viewing Angle	Horizontal	θ _{x+}	CR≥10	40	45	-	Deg.	
		θ _{x-}		40	45	-		
	Vertical	θ _{y+}		15	20	-		
		θ _{y-}		40	45	-		



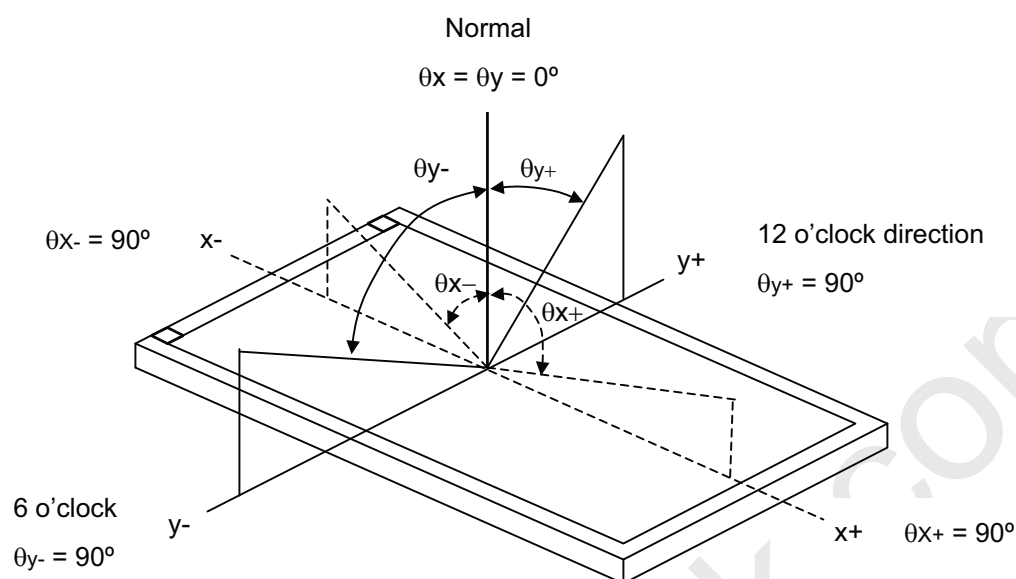
CHI MEI
OPTOELECTRONICS CORP.

Doc No.: 44082401
Issued Date: Aug. 08, 2008
Model No.: N141C6 - L01

Preliminary

www.panelook.com

Note (1) Definition of Viewing Angle (θ_x , θ_y):



Note (2) Definition of Contrast Ratio (CR):

The contrast ratio can be calculated by the following expression.

$$\text{Contrast Ratio (CR)} = L_{63} / L_0$$

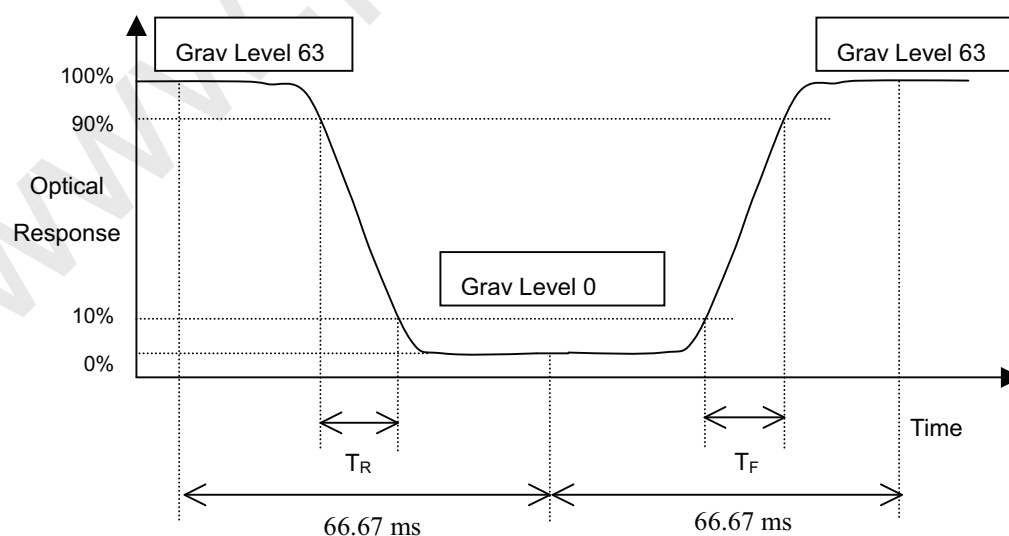
L63: Luminance of gray level 63

L 0: Luminance of gray level 0

$$\text{CR} = \text{CR} (5)$$

CR (X) is corresponding to the Contrast Ratio of the point X at Figure in Note (5).

Note (3) Definition of Response Time (T_R , T_F):



Note (4) Definition of Average Luminance of White (L_{AVE}):

Measure the luminance of gray level 63 at 5 points

$$L_{AVE} = [L(33) + L(37) + L(55) + L(73) + L(77)] / 5$$

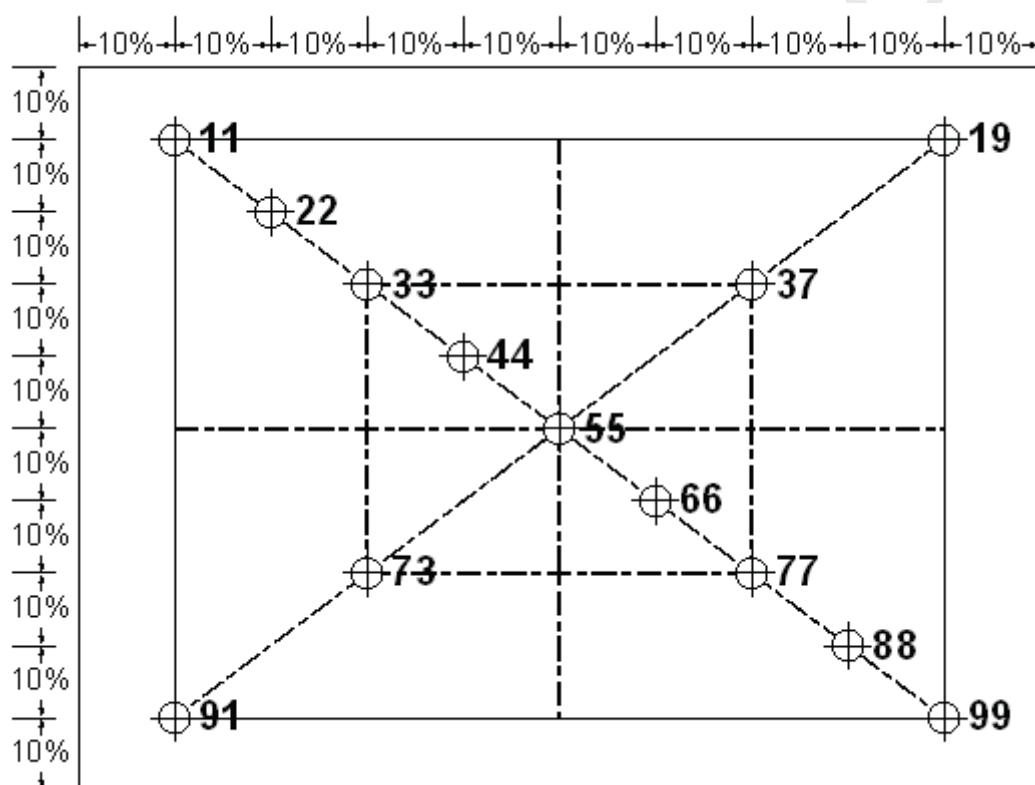
$L(x)$ is corresponding to the luminance of the point X at Figure in Note (5)

Note (5) Definition of White Variation (δW_{5p} , δW_{13p}):

Measure the luminance of gray level 63 at 5, 13 points

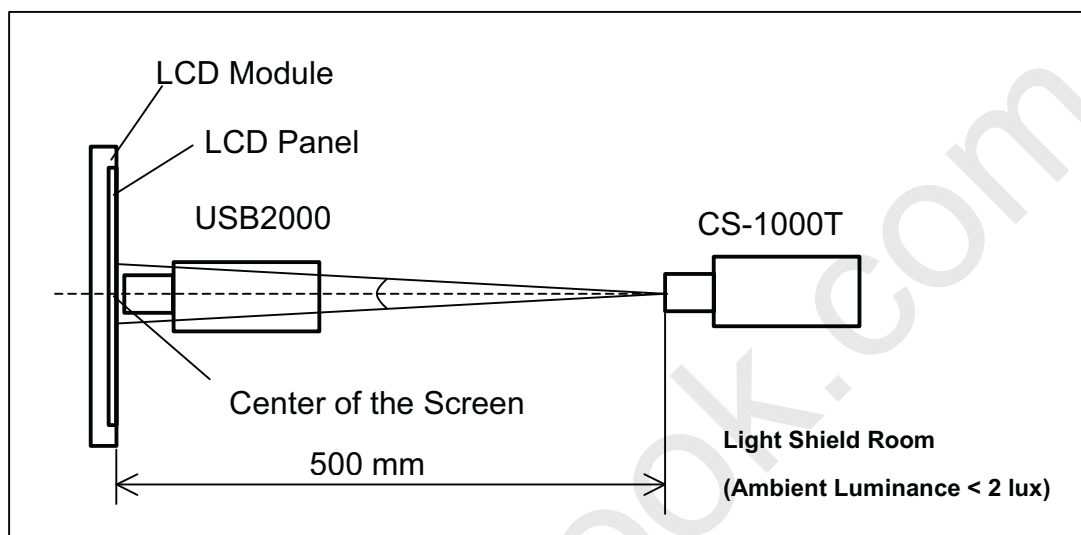
$$\delta W_{5p} = \{1 - [\text{Minimum } [L(33) + L(37) + L(55) + L(73) + L(77)] / \text{Maximum } [L(33) + L(37) + L(55) + L(73) + L(77)]]\} * 100\%$$

$$\delta W_{13p} = \{1 - [\text{Minimum } [L(11) \sim L(99)] / \text{Maximum } [L(11) \sim L(99)]]\} * 100\%$$



Note (6) Measurement Setup:

The LCD module should be stabilized at given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting Backlight for 20 minutes in a windless room.

**Note (7) Definition of color gamut (C.G):**

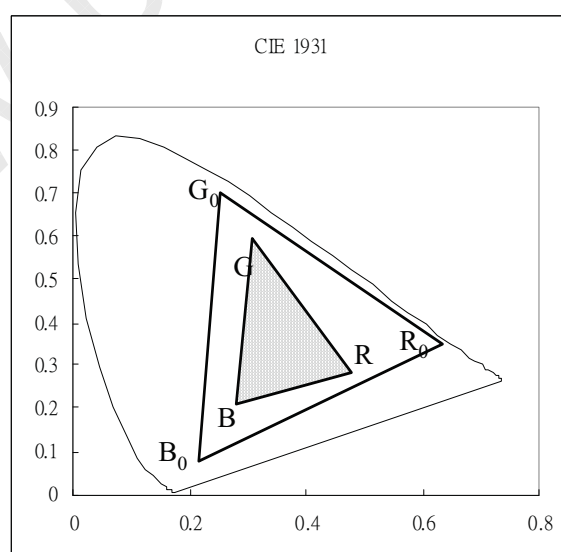
$$C.G = R G B / R_0 G_0 B_0 \cdot 100\%$$

R_0, G_0, B_0 : color coordinates of red, green, and blue defined by NTSC, respectively.

R, G, B : color coordinates of module on 63 gray levels of red, green, and blue, respectively.

$R_0 G_0 B_0$: area of triangle defined by R_0, G_0, B_0

$R G B$: area of triangle defined by R, G, B



8 PRECAUTIONS

8.1 ASSEMBLY AND HANDLING PRECAUTIONS

- (1) The module should be assembled into the system firmly by using every mounting hole. Be careful not to twist or bend the module.
- (2) While assembling or installing modules, it can only be in the clean area. The dust and oil may cause electrical short or damage the polarizer.
- (3) Use fingerstalls or soft gloves in order to keep display clean during the incoming inspection and assembly process.
- (4) Do not press or scratch the surface harder than a HB pencil lead on the panel because the polarizer is very soft and easily scratched.
- (5) If the surface of the polarizer is dirty, please clean it by some absorbent cotton or soft cloth. Do not use Ketone type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanently damage the polarizer due to chemical reaction.
- (6) Wipe off water droplets or oil immediately. Staining and discoloration may occur if they left on panel for a long time.
- (7) If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contacting with hands, legs or clothes, it must be washed away thoroughly with soap.
- (8) Protect the module from static electricity, it may cause damage to the C-MOS Gate Array IC.
- (9) Do not disassemble the module.
- (10) Do not pull or fold the lamp wire.
- (11) Pins of I/F connector should not be touched directly with bare hands.
- (12) To avoid wireless noise interference, please keep the antenna away from LCD control board.

8.2 SAFETY PRECAUTIONS

- (1) High temperature or humidity may reduce the performance of module. Please store LCD module within the specified storage conditions.
- (2) It is dangerous that moisture come into or contacted the LCD module, because the moisture may damage LCD module when it is operating.
- (3) It may reduce the display quality if the ambient temperature is lower than 10 °C. For example, the response time will become slowly, and the starting voltage of lamp will be higher than the room temperature.

8.3 OPERATION PRECAUTIONS

- (1) Do not pull the I/F connector in or out while the module is operating.
- (2) Always follow the correct power on/off sequence when LCD module is connecting and operating. This can prevent the CMOS LSI chips from damage during latch-up.
- (3) The startup voltage of Backlight is approximately 1000 Volts. It may cause electrical shock while assembling with inverter. Do not disassemble the module or insert anything into the Backlight unit.

9 PACKAGING

9.1 CARTON

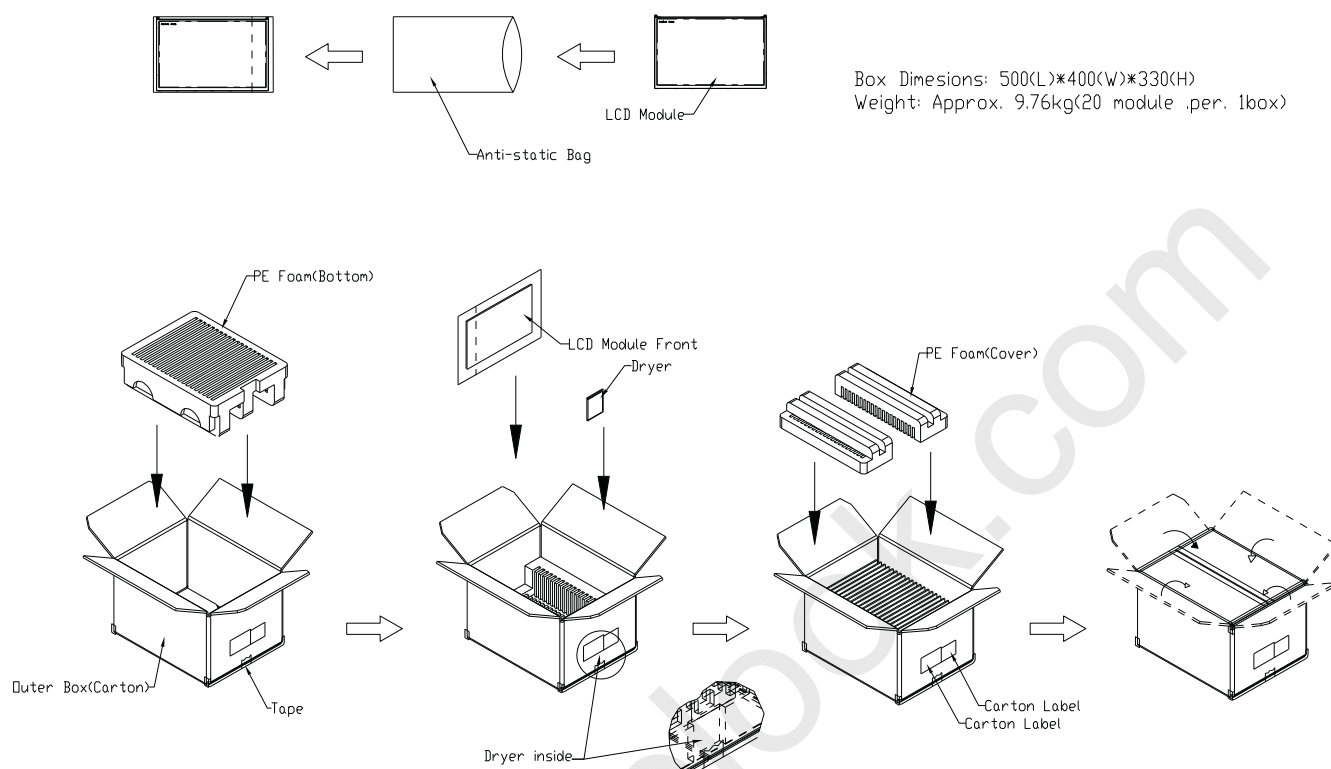
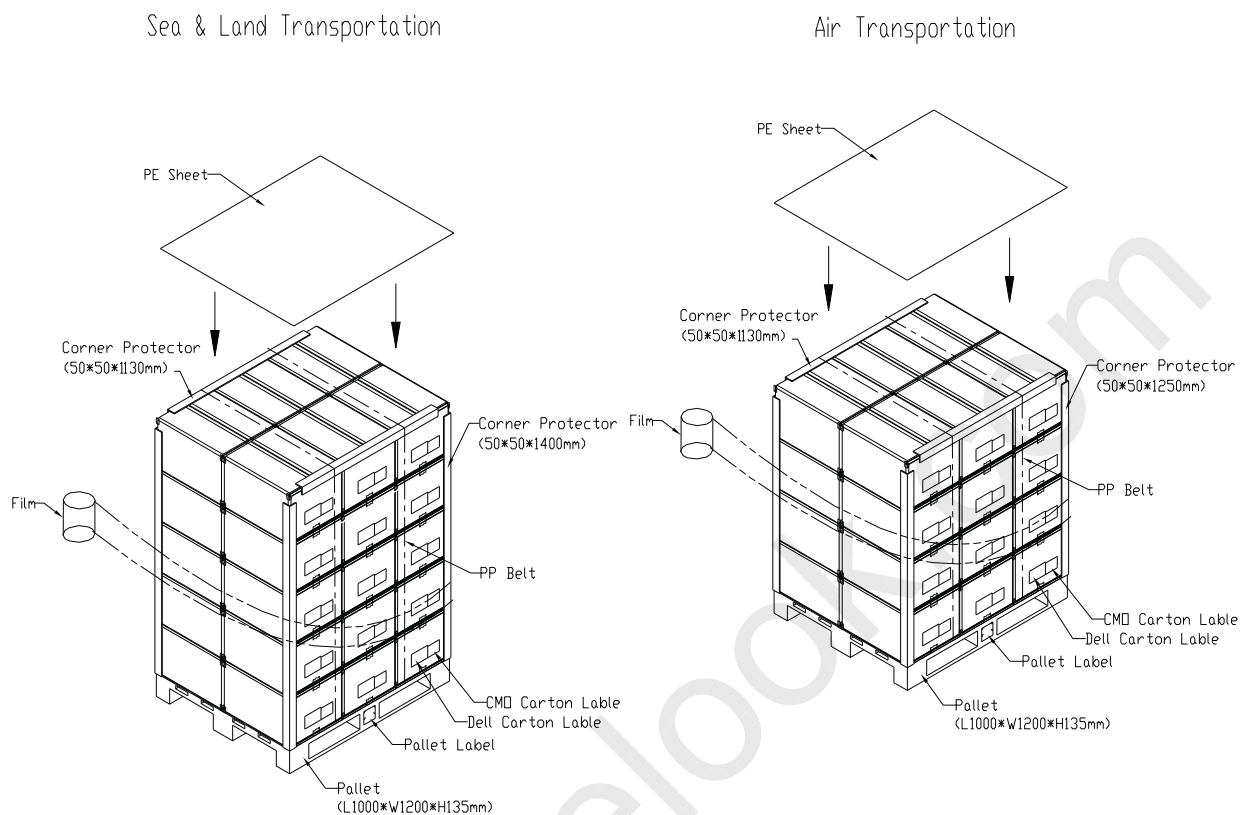


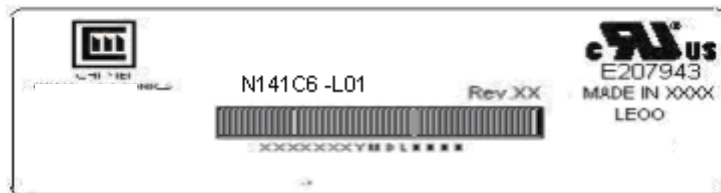
Figure. 9-1 Packing method

9.2 PALLET**Figure. 9-2 Packing method**

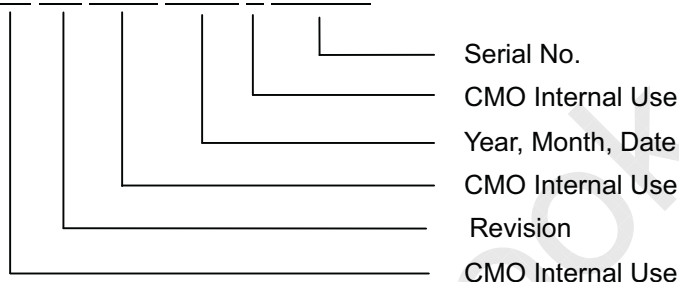
10 DEFINITION OF LABELS

10.1 CMO MODULE LABEL

The barcode nameplate is pasted on each module as illustration, and its definitions are as following explanation.



- (a) Model Name: N141C6 - L01
- (b) Revision: Rev. XX, for example: A1, ..., C1, C2 ...etc.
- (c) Serial ID: X X X X X X X Y M D X N N N N



- (d) Production Location: MADE IN XXXX. XXXX stands for production location.
- (e) UL/CB logo: "LEOO" especially stands for panel manufactured by CMO Ningbo satisfying UL/CB requirement. "LEOO" is the CMO's UL factory code for Ningbo factory.

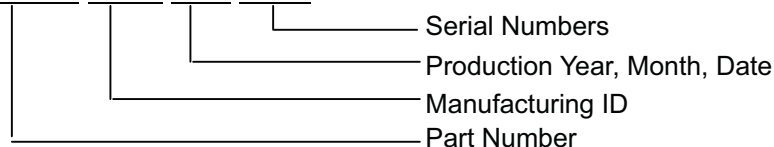
Serial ID includes the information as below:

- (a) Manufactured Date: Year: 1~9, for 2001~2009
 Month: 1~9, A~C, for Jan. ~ Dec.
 Day: 1~9, A~Y, for 1st to 31st, exclude I, O and U
- (b) Revision Code: cover all the change
- (c) Serial No.: Manufacturing sequence of product

Dell PPID label contains information as below:



- (a) Serial ID: TW-0SSSSS-70896-YMD-XXXX



- (b) Production location: Made in XXXX.
- (c) Revision code: X00, X10, X20, A00..etc.

10.2 CMO CARTON LABEL



CHI MEI OPTOELECTRONICS

PO.NO. _____

Part ID. _____

Model Name _____

Carton ID. _____ Quantities _____

Made In XXXX

GP RoHS

(a) Production location: Made In XXXX. XXXX stands for production location.

10.3 CARTON LABEL

PKG ID (3S)124161241729112345609886C20 		 REV.A06
DP/N 03J849 	 Vendor ID Loc Id 12416 12416	
BOX Qty 20 	Made in Taiwan 	 Mfg Id 70896

Type J Label

- Verdana font or equivalent,bold
- 20pt.-all fields
- 203 DPI printer minimum
- Code 128B
- 10-15 mil minimum narrow bar
- .75"minimum barcode height
- .10" or greater quiet zone
- 4.0" x 6.0" label size
- Brady THT -25-402-1 or equivalent
- Brady R6107 series ribbon or equivalent

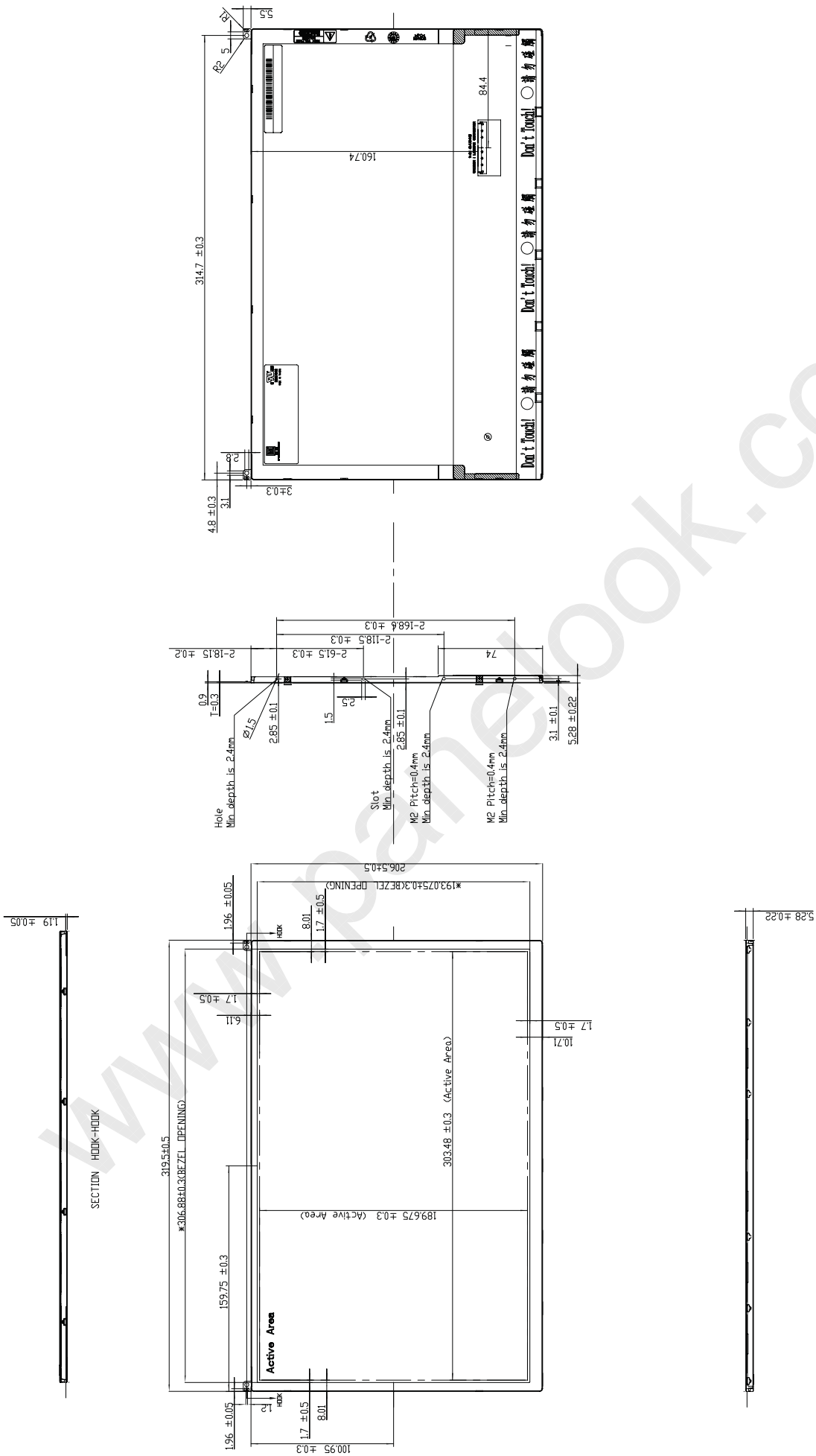


10.4 PALLET LABEL

FROM :CMO Corporation Tainan, Taiwan 744 R.O.C		TO:DELL COMPUTER 2128 West Braker Austin TX	
P.O.NUMBER 12345678			
		DELL P/N 12345	
COUNTRY OF ORIGIN TW			
		PACKING LIST# 1234567890123	
PACKING LIST QTY 654321			
		DESTINATION MAS LOC 60	
DESTINATION LOCATION B4			
AIRBILL NUMBER 12345678901234567890			
			
PKG CNT 999 OF 999	BOX CNT 12345	REVISION A00-00	SHIP DATE Apr 29,2003
PART DESCRIPTION XXXXXXXXXXXXXXXXXXXXXXXX 12345678901234567890123456789012345678901			

Type K Label

- Verdana font or equivalent,bold
- 12pt.-all descript fields
- 10pt.-all data fields
- 203 DPI printer minimum
- Code 128B
- 10 mil minimum narrow bar
- .30-.50"minimum barcode height
- .10" or greater quiet zone
- 4.0" x 6.5" label size
- Brady THT -78-402-.9 or equivalent
- Brady R6107 series ribbon or equivalent



NOTES:
1. MAX. SCREW LENGTH: 2.5mm.
2. MAX. SCREW TORQUE: 2.0 kgf-cm.
3. FPC CONNECTOR: 59453-09110EDLF (FCL).
4. LCD MODULE INPUT CONNECTOR: FT-VHP50S-A-H11C(AE).
5. **MARKS THE DESIGN CRITICAL DIMENSIONS.
6. *Ø MARKS THE PROCESS CRITICAL DIMENSIONS.

TITLE		PART NAME		DRAWING NO.		REVISION	
Approved		Bill		Drawing		Part No.	
Described		Drawing		Part No.		Part No.	
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